IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application Inventor(s): Laptev, P. Appln. No.: 09/829,587 Confirm. No.: 7932 Filed: April 9, 2001 Title: SYSTEM FOR, AND METHOD OF, ETCHING A SURFACE ON A WAFER	PATENT APPLICATION Art Unit: 1792 Examiner: Zervigon, R. **Customer No. 23910**

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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SIXTH SUPPLEMENTAL APPEAL BRIEF

Sirs:

Appellant submits this Brief for consideration by the Board of Patent Appeals and Interferences following the Notification of Non-Compliant Brief under 37 CFR 41.37 mailed on October 23, 2007. Appellant submitted a Notice of Appeal along with the appropriate fee on October 9, 2003.

I. REAL PARTY IN INTEREST

Sputtered Films, Inc., the assignee of record of the application.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-21 and 43-51 have been rejected by the Examiner on the basis of prior art cited by the Examiner. Claims 22-42 have been withdrawn from prosecution in the application. Claims 1-51 have been, and are, the only claims in the application. The rejection of claims 1-21 and 43-51 is being appealed.

IV. STATUS OF AMENDMENTS

Applicant filed a proposed amendment under Rule 116 on October 30, 2003 to amend one (1) word in each of claims 1, 3, 8, 48 and 49, so as to make the claims consistent with the disclosure in the specification and the drawings. In an Office Action dated 11/07/2003, the Examiner refused to enter the proposed amendment on the ground that applicant's amendment to claim 3 changing "less" to -- greater -- "requires additional consideration of the cited prior art." Applicant has accordingly written claims 1, 3, 8, 48 and 49 in this Supplemental Appeal Brief without including applicant's proposed changes in the claims.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The following detailed summary correlates features of the independent claims on appeal with excerpts from the Specification using numbered footnotes. The correlations include figure reference numerals inserted into the text of the claims and are necessarily drawn to particular embodiments. It should be noted that the claims are not intended to be restricted to the particular embodiments correlated to the features, but rather the excerpts and labeling provided are merely intended to demonstrate support for the claims within the Specification and to guide the Appeal process.

Independent claims 1, 7, 14 and 21 (as presented in the appeal) are listed first with superscripted numerals appearing within the claims and corresponding to Footnotes 1-6, which follow and identify support from the specification by page and line number.

1. In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition, a conduit for molecules of an inert gas,

a first electrode **(24, Fig. 1)** biased to a first voltage[1] and spaced **(**see space between **22** and **16, Fig. 1)** from the wafer **(16, Fig. 1)**,

a second electrode **(22, Fig. 1)** biased to a second voltage[2] lower than the first voltage and spaced[3] from the first electrode **(24, Fig. 1)** and the wafer **(16, Fig. 1)** and further spaced from the wafer **(16, Fig. 1)** than the first electrode **(24, Fig. 1)**,

magnetic members **(26,28, Fig. 1)** providing a magnetic field,

the first electrode **(24, Fig. 1)** and the magnetic members **(26,28, Fig. 1)** being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas[4], and

the second electrode **(22, Fig. 1)** and the wafer **(16, Fig. 1)** being disposed relative to each other and to the ions of the inert gas, and the second electrode **(22, Fig. 1)** being constructed, to obtain a movement of the ions to the wafer **(16, Fig. 1)** at a low and controlled speed for an etching of the surface of the insulating layer **(12, Fig. 1)** by the ions at a low and controlled speed.[5]

7. In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

an enclosure **(20, Fig. 1)** defined by magnetic members **(26,28, Fig. 1)** forming a magnetic field and by first **(24, Fig. 1)** and second electrodes **(22, Fig. 1)** spaced from each other and from the wafers **(16, Fig. 1)** [3] and providing electrical fields **(36,40, Fig. 1)**,

a supply of molecules of an inert gas **(45, Fig. 1)** for introducing the molecules into the enclosure **(20, Fig. 1)**,

a first source of an alternating voltage **(40, Fig. 1)** for producing a direct negative voltage of a high magnitude on the first electrode **(24, Fig. 1)** for the creation of a first electrical field of a high magnitude in the enclosure **(20, Fig. 1)** [1],

a second source of an alternating voltage **(36, Fig. 1)** for producing a direct negative voltage of a low magnitude on the second electrode **(22, Fig. 1)** for the creation of a second electrical field of a low magnitude in the enclosure **(20, Fig. 1)** [2],

the molecules of the inert gas **(45, Fig. 1)** in the enclosure **(20, Fig. 1)** being ionized by the combination of the electrical and magnetic fields[4], and

the wafer **(16, Fig. 1)** being disposed relative to the second electrode **(22, Fig. 1)** and relative to the ions of the inert gas in the enclosure **(20, Fig. 1)** to receive an etching of a low magnitude on the surface of the insulating layer by the ions of the inert gas **(45, Fig. 1)** in the enclosure **(20, Fig. 1)**. [5]

14. In combination for etching an insulating layer in a wafer disposed in an enclosure to present a clean and fresh surface on the insulating layer for deposition,

magnetic members **(26,28, Fig. 1)** defining a magnetic field in the enclosure,

a first source of an alternating voltage **(36, Fig. 1)** for providing a first electrical field of a high magnitude in the enclosure **(20, Fig. 1)** [1],

a first electrode **(24, Fig. 1)** forming a part of the enclosure **(20, Fig. 1)** and connected to the first source of voltage **(40, Fig. 1)** for providing a negative DC voltage of a relatively high magnitude at a first position in the enclosure **(20, Fig. 1)** [1],

a second source of an alternating voltage **(40, Fig. 1)** for providing a second electrical field of a low magnitude in the enclosure **(20, Fig. 1)** [2],

a second electrode **(22, Fig. 1)** forming a part of the enclosure **(20, Fig. 1)** and connected to the second source of the alternating voltage **(36, Fig. 1)** for providing a negative DC voltage of a relatively low magnitude at a second

position displaced from the first position and the wafer **(16, Fig. 1)** but near the wafer **(16, Fig. 1)** [2,3],

a conduit **(44, Fig. 1)** for introducing molecules of an inert gas **(45, Fig. 1)** into the enclosure **(20, Fig. 1)** for ionization by the combination of the electrical and magnetic fields to produce ions of high density[4],

the second electrode **(22, Fig. 1)** and the wafer **(16, Fig. 1)** providing a first capacitor of a high impedance, and the wafer and the ions in the enclosure **(20, Fig. 1)** providing a second capacitor of a low impedance, in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer **(12, Fig. 1)** in the wafer **(16, Fig. 1)**. [6]

21. In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure **(20, Fig. 1)**

first **(24, Fig. 1)** and second **(22, Fig. 1)** electrodes disposed in the enclosure **(20, Fig. 1)** and displaced from each other and from the wafer **(16, Fig. 1)** for producing electrical fields in the enclosure **(20, Fig. 1)**, and

magnetic members **(26,28, Fig. 1)** disposed in the enclosure **(20, Fig. 1)** for producing a magnetic field in the enclosure **(20, Fig. 1)** in a direction transverse to the electrical field,

a first voltage source **(40, Fig. 1)** for producing a voltage of a high magnitude in the vicinity of the first electrode **(24, Fig. 1)** to obtain a production of a high electrical field in the enclosure **(20, Fig. 1)** [1],

a second voltage source **(36, Fig. 1)** for producing a voltage of a low magnitude in the vicinity of the second electrode **(22, Fig. 1)** to obtain a production of a low electrical field in the enclosure **(20, Fig. 1)** [2], and

a supply **(45, Fig. 1)** of molecules of an inert gas for introduction into the enclosure **(20, Fig. 1)** to cooperate with the first **(24, Fig. 1)** and second **(22, Fig. 1)** electrodes and the magnetic members **(26,28, Fig. 1)** in obtaining an ionization of the gas molecules in the enclosure **(20, Fig. 1)** by the electrical and magnetic fields in the enclosure **(20, Fig. 1)** and in

obtaining a movement of the ions in the enclosure **(20, Fig. 1)** to the insulating layer **(12, Fig. 1)** in the wafer **(16, Fig. 1)** at a speed to obtain a smooth and uniform etching of the surface of the insulating layer **(12, Fig. 1)** at a low rate without any pits in the surface of the insulating layer **(12, Fig. 1)**. [4,5]

Footnotes:

1. Specification page 4, lines 11-15, including:

> "The first electrode is biased at a high negative voltage by a high alternating voltage to produce a high intensity electrical field."

2. Specification page 4, lines 11-15, including:

> "The first electrode is biased **at a high negative voltage** by a high alternating voltage to produce a high intensity electrical field. The second electrode is biased **at a low negative voltage** by a low alternating voltage to produce a low intensity electrical field. Electrons movable in a helical path in the enclosure near the first electrode ionize inert gas molecules" (Emphasis added).

3. Specification page 4, lines 16 to page 5, lines 1-4, including:

> "A wafer having a floating potential and having an insulating layer is closely **spaced from the second electrode**. The electrode and the wafer define plates of a first capacitor having a dielectric formed by inert gas molecules and ions between the plates to provide a high impedance. The wafer and the gas ions in the enclosure define opposite plates of a second capacitor, in series with the first capacitor, having the insulating layer as the dielectric to define a low impedance" (Emphasis added).

Specification page 8, lines 1-10, including:

> "The electrode 22 is disposed in a contiguous and substantially parallel relationship to the wafer 16 and is movable in position toward or away

from the wafer, as indicated by a double-headed arrow 25. **The spacing between the wafer 16 and the electrode 22 may illustratively be in the order of 0.1-2 mm.** A plate 30 extending from the magnet 26 in a substantially parallel, but spaced, relationship to the electrode 22 also defines the enclosure 20. A ring 32 extending from the magnet 28 to a position spaced from, but contiguous to, the electrode 24 also defines in part the enclosure 20" (Emphasis added).

Specification page 13, lines 14-18, including:

"As previously indicated, **the wafer 16 is separated from the electrode 22** in the preferred embodiment 10 of this invention. **The separation may be in the order of 0.1 to 2.0 millimeters**, This causes two (2) capacitors 52 and 54 in FIG. 4b to be defined by the electrode 22, the wafer 16 and the charge produced by the argon ions 51 in the enclosure 20 in the vicinity of the electrode 22."

4. Specification page 4, lines 11-15, including:

"The first electrode is biased at a high negative voltage by a high alternating voltage to produce a high intensity electrical field. The second electrode is biased at a low negative voltage by a low alternating voltage to produce a low intensity electrical field. **Electrons movable in a helical path in the enclosure near the first electrode ionize inert gas molecules**" (Emphasis added).

5. Specification page 10, lines 6-17, including:

"A negative bias is produced on the electrode 22 because of the alternating voltage applied to the electrode. In the positive half cycles of the alternating voltage, the electrode 22 attracts electrons because of the electrical field between the electrode and the ground potential 34 on the plate 30. In the negative half cycles of the alternating voltage, positive ions are attracted to the electrode because of the electrical field between the electrode and the ground potential 34 on the plate 30. **Since the**

electrons are considerably lighter in weight than the positive ions, they move faster toward the electrode 22 than the positive ions. This causes the electrons to accumulate in the space adjacent the electrode 22, thereby producing the negative DC bias on the electrode. The electrode 24 receives a negative bias because of the same physical phenomenon. However, **the negative bias on the electrode 22 is considerably less than the negative DC bias on the electrode 24** because of the differences in the voltages applied to the electrodes" (Emphasis added).

6. Specification page 4, lines 16 to page 5, lines 1-4, including:

"A wafer having a floating potential and having an insulating layer is closely spaced from the second electrode. The electrode and the wafer **define plates of a first capacitor** having a dielectric formed by inert gas molecules and ions between the plates to provide a high impedance. The wafer and the gas ions in the enclosure **define opposite plates of a second capacitor**, in series with the first capacitor, having the insulating layer as the dielectric to define a low impedance" (Emphasis added).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Examiner has provided the grounds of rejection as follows:

A. Rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 under 35 U.S.C. 102(b) as being anticipated by Koshimizu (U.S. Patent 5,980,687) and demonstrated by Mountsier (U.S. Patent 5,810,933).

B. Rejection of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49, and 51 under 35 U.S.C 103(a) as being unpatentable over Koshimizu (U.S. Patent 5,980,687) in view of Mountsier (U.S. Patent 5,810,933).

C. Rejection of claims 1-21, and 43-51 under 35 U.S.C 103(a) as being unpatentable over Applicant's own admitted prior art in view of Mountsier (U.S. Patent 5,810,933).

VII. ARGUMENT IN RESPONSE TO REJECTIONS.

A. Rejection of claims 1-4, 7-9, 11, 14-16, 19-21, 43-47, and 50 under 35 U.S.C. 102(b) as being anticipated by Koshimizu (5,980,687) and demonstrated by Mountsier et al. (5,810,933).

Applicant submits that the invention disclosed in the present application is the separation of the electrodes and the wafer, which provides a smoother surface on the wafer after etching.

Applicant submits that Koshimizu does not provide a separation between the electrodes and the wafer. Figs. 1 and 3 of Koshimizu clearly show that the wafer W is either attached to the electrode 116 or attached to the electrode 110. Further, Koshimizu also discloses that the wafer W is fixed on the surface of either electrode 110 or 116:

"As a result, the wafer W fixed on the first susceptor 110 can be kept at a predetermined temperature", col. 3, lines 64-66;

"Cramp means ... is provided on the wafer mounting or supporting surface of the first susceptor 110 for enabling the wafer W to be fixed on the susceptor in a desired state", col. 3. lines 66-67 to col. 4, lines 1-3; and

"A second susceptor 116 which constitutes an upper electrode and can fix a wafer W thereon..." col. 4, lines 8-9.

Further, the Examiner also states that the wafer W is attached to either electrode 110 or 116.

Since Koshimizu discloses two wafers W, one might argue that the top wafer (as shown in Fig. 1 or Fig. 3) is separated from the bottom electrode 110, and the bottom wafer W is separated from the top electrode 116. But this argument does not show the separation of one wafer from both electrodes, which is the inventive idea of the present application.

Thus applicant submits that the present disclosure of the separation between the electrodes and the wafer is not anticipated by Koshimizu.

With respect to the demonstration by Mountsier et al., the Examiner states that:

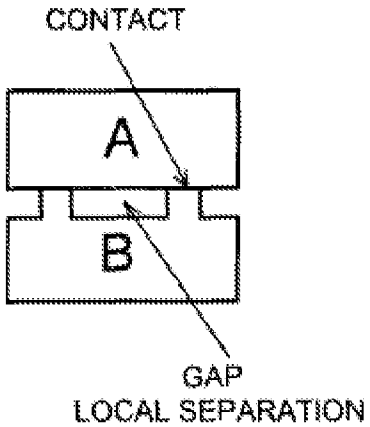
"it is anticipated by Koshimizu and common practice in the art that all wafers (or other articles) positioned on supports or electrodes would necessarily have a gap between the wafer/article and the support surface upon which the wafer/article is resting or electrically clamped and where providing a direct current bias as a result of the first (134) and second (130) sources of alternating voltage." Underlined provided by applicant.

Applicant submits that *"have a gap"* is different from *"separation"*.

- "*Separation* between a wafer and a support" means that the wafer and the support do not contact at any point. In other words, *"separation"* means there is no contacting point at all at the wafer-support interface. Generally speaking, separation between two articles implies a complete separation between these two articles.

- "*Have a gap"* means that there exists some local separations, meaning that there are some locations at the wafer-support interface where the wafer surface and the support surface are separated. Thus it is possible for a wafer and a support to *have a gap* between them but they are *not separated.*

In other words, A and B are separated also means that A and B have a gap between them. But the reverse is not necessarily true. A and B have a gap between them does not necessarily means that A and B are separated. The following figure illustrates this point.



The situation also is demonstrated by Mountsier et al. Mountsier et al. shows that there is a gap between the wafer and the support, but Mountsier et al. also shows that

there is some contact between them (Fig. 6, interface between 62 and 52). Thus the wafer 62 and the support 52 have a gap between them, but they are not separated.

Thus applicant agrees with the Examiner that there is always a gap (at least in the microscopic scale) between the wafer and the support, but respectfully submits that this does not indicate nor imply that the wafer and the support are separated as disclosed in the present application.

Thus applicant submits that it is not anticipated by Koshimizu, nor it is a common practice in the art that a wafer is positioned on a support or an electrode in such as way so that the wafer and the support/electrode surface upon which the wafer is resting or electrically clamped are separated. The wording of support, resting, or clamp normally implies a contact between the two objects.

In summary, for the rejection of these claims as a group, applicant submits that Koshimizu does not disclose a separation between the wafer and the electrodes, and Mountsier et al. demonstrates that it is common practice that there exists a gap between the wafer and the electrode, but Mountsier et al. also demonstrates that the wafer and the electrode are not separated.

With respect to the individual claims, applicant submits that:

Claim 1: Claim 1 provides

"...a wafer...

a first electrode…spaced from the wafer.

a second electrode…spaced from the wafer…"

Applicant submits that the claim language of "spaced from", together with the specification language of "separation", means that the wafer is spaced from the two electrodes, that the wafer is separated from the two electrodes, and that the wafer does not possess any contact point with the two electrodes.

Therefore as per the above argument, claim 1 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claim 7: Claim 7 provides

"...a wafer...

...first and second electrodes spaced from each other and from the wafer..."

Applicant submits that the claim language of "spaced from", together with the specification language of "separation", means that the wafer is spaced from the two electrodes, that the wafer is separated from the two electrodes, and that the wafer does not possess any contact point with the two electrodes.

Therefore as per the above argument, claim 7 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claim 8: Claim 8 provides:

"...the first electrode being disposed in contiguous, but spaced, relationship to the wafer."

Applicant submits that the language of "spaced relationship", together with the specification language of "separation", means that the wafer is spaced from the first electrode, that the wafer is separated from the first electrode, and that the wafer does not possess any contact point with the first electrode.

Therefore as per the above argument, taken together with claim 7, claim 8 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claim 11: Claim 11 provides:

"...the wafer being disposed in a spaced, but adjacent, relationship to the second electrode…"

Applicant submits that the language of "spaced relationship", together with the specification language of "separation", means that the wafer is spaced fiom the second electrode, that the wafer is separated from the second electrode, and that the wafer does not possess any contact point with the second electrode.

Therefore as per the above argument, taken together with claim 7, claim 11 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claim 14: Claim 14 provides:

"...the second electrode and the wafer providing a first capacitor…"

Applicant submits that for the second electrode and the wafer to form a capacitor, they have to be separated, not just having a gap, since any contact point would electrically connect the electrode and the wafer, and thus forming a conductor, not a capacitor.

Therefore as per the above argument, claim 14 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claim 20: Claim 20 provides

"...the wafer having a floating potential…"

Applicant submits that for the wafer to have a floating potential, the wafer has to be separated from both electrodes, since a contact with an electrode will provide the wafer with the potential of that electrode.

Therefore as per the above argument, taken together with claim 14, claim 20 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claim 21: Claim 21 provides:

"...a wafer...

...first and second electrodes displaced from each other and from the wafer…"

Applicant submits that the language of "displaced from each other" and "displaced from the wafer", together with the specification language of "separation", means that the wafer is displaced from the two electrodes, that the wafer is separated from the two electrodes, and that the wafer does not possess any contact point with the two electrodes.

Therefore as per the above argument, claim 21 is not anticipated by Koshimizu, even with the demonstration by Mountsier et al.

Claims 2-4, 9, 15-16, 19,43-47, and 50: These claims are dependent on other independent claims.

B. Rejection of claims 5,6,10,12,13,17,18,20,48,49 and 51 under 35 U.S.C. 103(a) as being unpatentable over Koshimizu (5,980,687) in view of Mountsier et al. (5,810,933).

- These are dependent claims, therefore applicant submits that these claims would be allowed if the argument presented above in A (rejection based on 35 U.S.C. 102(b)) is successful.

- In the event that the argument presented in A is not successful, applicant submits two arguments against this rejection.

1. There is no motivation nor suggestion for Koshimizu to replace his wafer support platform with Mountsier et al.'s wafer support platform.

The Examiner states that the motivation is to provide an alternate means for supporting the substrate.

Applicant submits that the present invention is based on the discovery that the separation of the wafer from the electrodes provides a smoother etch surface for the wafer. Thus applicant submits that it would not be obvious to persons with ordinary skills in the art to connect the idea of an alternate means for supporting the substrate to the present invention of achieving a smoother wafer surface after etching.

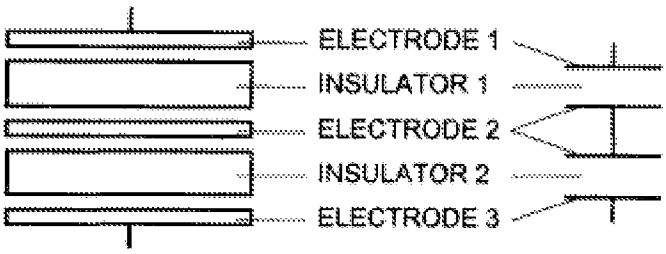
In other words, applicant submits that replacing Koshimizu's wafer support platform with Mountsier et al.'s wafer support platform to achieve a smoother wafer surface after etching can only be obvious after the disclosure of the present invention, since there is neither teaching nor suggestion that the replacement would affect the wafer surface or the process performance.

Thus applicant submits that the rejection based on the combination of Koshimizu and Mountsier et al. is improper, since there is no motivation, nor teaching or suggestion linking the process performance enhancement between these two references, and the stated motivation from the Examiner does not provide the necessary connection.

2. Mountsier et al. does not disclose a series relationship between two capacitors.

In one embodiment, applicant discloses a series relationship between two capacitors. To have a construction of two capacitors in series, there needs to be three

electrodes (electrode 1, electrode 2, and electrode 3) and two insulators (insulator 1, and insulator 2) with the insulator 1 disposed between electrodes 1 and 2, and the insulator 2 disposed between electrodes 2 and 3. See the following drawing.



In this embodiment, applicant discloses that the electrode 1 is the electrode 22 (of Fig. 3, or 4a or 4b), electrode 2 is the wafer 16 (of Fig. 3, or 4a or 4b), and electrode 3 is the accumulation of charges 5 1 (of Fig. 3, or 4a or 4b). The insulator 1 is the space between electrode 22 (of Fig. 3, or 4a or 4b), electrode 2 is the wafer 16 (of Fig. 3, or 4a or 4b), and the insulator 2 is the dielectric layer deposited on the wafer 16 (of Fig. 3, or 4a or 4b).

In contrast, Mountsier et al. does not disclose a wafer with a dielectric layer, thus there is no insulator 2, and therefore no capacitor #2. There is only one capacitor formation disclosed in Mountsier et al., where electrode 1 is the metallic support disk 56 (col. 2, lines 57-61, col. 4, lines 39-40), insulator 1 is the ceramic disk 52, and electrode 2 is the wafer 62. Applicant submits that the two capacitors stated by the Examiner is indeed only one capacitor, since the "68 dielectric gap; Fig. 5, col. 4, lines 20-23" and "80182 dielectric gap, Fig. 6" are two part of an insulator located between two electrodes 56 (metallic support disk) and 62 (wafer).

Thus applicant submits that Mountsier et al. discloses only one capacitor formation.

C. Rejection of claims 1-21'43-51 under 35 U.S.C. 103(a) as being unpatentable over Applicant's own admitted prior art in view of Mountsier et al. (5,810,933).

Applicant submits that the invention disclosed in the present application is the separation of the electrodes and the wafer, which provides a smoother surface on the wafer after etching. Applicant submits that the invention is patentable in view of Mountsier et al.

Similar to the argument against the rejection in B (rejection under 35 U.S.C. 103(a)), applicant submits two arguments against this rejection.

1. There is no motivation, nor teaching or suggestion for one with ordinary skill in the art at the time the invention was made for the using of Mountsier et al.'s wafer support platform with Applicant's own admitted prior art.

(The Examiner states that:

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Koshimizu to replace his wafer support platform with Mountsier's wafer support platform,

Motivation for Koshimizu to replace his wafer support platform with Mountsier's wafer support platform is to provide an alternate means for supporting the substrate.

Underlined provided by applicant.

Applicant assumes that the reference to Koshimizu is a typo, and it should be replaced with the reference to Applicant's own admitted prior art. If the assumption is incorrect, then the argument in B above applies).

Applicant submits that the present invention is based on the discovery that the separation of the wafer from the electrodes provides a smoother etch surface for the wafer. Mountsier et al.'s wafer support platform is disclosed to be a wafer cooling device (WCD), designed for cooling a substrate. Thus applicant submits that it would not be obvious to persons with ordinary skills in the art to connect the idea of an alternate means for supporting the substrate, or an innovated wafer cooling device for supporting a substrate to the present invention of achieving a smoother wafer surface after etching.

In other words, applicant submits that using Mountsier et al.'s wafer support platform with existing etch process technology to achieve a smoother wafer surface after

etching can only be obvious after the disclosure of the present invention, since there is neither teaching nor suggestion that the replacement would affect the wafer surface or the process performance.

Thus applicant submits that the rejection based on the combination of Applicant's own admitted prior art and Mountsier et al. is improper, since there is no motivation, nor teaching or suggestion linking the process performance enhancement between these two references, and the Examiner's stated motivation of providing an alternate means for supporting the substrate does not provide the necessary connection.

2. Mountsier et al. does not disclose a series relationship between two capacitors.

Similar to the argument presented above in B, applicant submits that Mountsier et al. discloses only one capacitor formation, in contrast to an embodiment of the present invention presenting two capacitors in series.

Further, the rejection based on two capacitors in series only applies to claims 11, 13, 14-20, 48, 49 and does not apply to claims 1-10, 12, 21, 43-47, 50-51 since the latter claims do not involve with the formation of capacitor. Further, the use of a perfectly insulated ceramic covering the electrode would cause the wafer to be electrically floated, and therefore only the claims 5, 6, 10, 17 involved with floating potential are affected. And thus the rejection based on capacitors and wafer floating potential does not affect claims 1-4, 7-9, 12, 21, 43-47 and 50-51.

VIII. CONCLUSION AND RELIEF

Based on the foregoing, Applicant requests that the Board overturn the Examiner's rejection of all pending claims and hold that the claims of the present application are allowable.

The Commissioner is hereby authorized to charge any deficiencies or credit overpayment to Deposit Account No. 06-1325.

Respectfully submitted,

Dated: November 14, 2007

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IX. CLAIMS APPENDIX.

Claims on Appeal:

1. (Previously Presented) In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition, a conduit for molecules of an inert gas,

a first electrode biased to a first voltage and spaced from the wafer,

a second electrode biased to a second voltage lower than the first voltage and spaced from the first electrode and the wafer and further spaced from the wafer than the first electrode,

magnetic members providing a magnetic field,

the first electrode and the magnetic members being disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas, and

the second electrode and the wafer being disposed relative to each other and to the ions of the inert gas, and the second electrode being constructed, to obtain a movement of the ions to the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at a low and controlled speed.

2. (Previously Presented) In a combination as set forth in claim 1,

a first member disposed adjacent the first electrode for providing a reference potential different from the bias on the first electrode to create a first electrical field, and

a second member disposed adjacent the second electrode for providing the reference potential to create a second electrical field,

the first electrical field and the magnetic field being disposed relative to each other and to the molecules of the inert gas from the supply for ionizing the molecules of the inert gas,

the second electrical field and the magnetic field being disposed relative to each other and to the ions of the inert gas to obtain the movement of the ions to the wafer at the low and controlled speed,

the second electrode being contiguous to, but spaced from, the wafer.

3. (Previously Presented) In a combination as set forth in claim 1,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the bias on the first electrode being less than the bias on the second electrode.

4. (Original) In a combination as set forth in claim 1,

the first electrode being disposed in a substantially parallel and contiguous relationship to the wafer,

there being a path for the flow of the argon molecules from the vicinity of the first and second electrodes and the magnetic members.

5. (Previously Presented) In a combination as set forth in claim 1,

the wafer being at a floating potential,

there being first and second electrically conductive members respectfully adjacent the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

6. (Previously Presented) In a combination as recited in claim 2,

a first source of alternating voltage for creating the bias on the first electrode, the bias on the first electrode being a negative direct voltage,

a second source of alternating voltage for creating the bias on the second electrode, the bias on the second electrode being a negative direct voltage,

the first electrode being disposed in a substantially parallel and contiguous relationship to the wafer,

there being a path for the flow of the molecules of the inert gas from the vicinity of the first and second electrodes and the magnetic members,

the wafer being at a floating potential,

there being first and second electrically conductive members respectfully adjacent, but spaced from, the first and second electrodes at a reference potential to provide for the creation of electrical fields respectively between the first electrode and the first electrically conductive member and between the second electrode and the second electrically conductive member.

7. (Previously Presented) In combination for etching an insulating layer in a wafer to present a clean and fresh surface on the insulating layer for deposition,

an enclosure defined by magnetic members forming a magnetic field and by first and second electrodes spaced from each other and from the wafers and providing electrical fields,

a supply of molecules of an inert gas for introducing the molecules into the enclosure,

a first source of an alternating voltage for producing a direct negative voltage of a high magnitude on the first electrode for the creation of a first electrical field of a high magnitude in the enclosure,

a second source of an alternating voltage for producing a direct negative voltage of a low magnitude on the second electrode for the creation of a second electrical field of a low magnitude in the enclosure,

the molecules of the inert gas in the enclosure being ionized by the combination of the electrical and magnetic fields, and

the wafer being disposed relative to the second electrode and relative to the ions of the inert gas in the enclosure to receive an etching of a low magnitude on the surface of the insulating layer by the ions of the inert gas in the enclosure.

8. (Previously Presented) In a combination as set forth in claim 7,

an opening in the enclosure for the flow of the molecules and ions of the inert gas from the enclosure,

the first source of the alternating voltage being operative to produce a direct voltage of the high magnitude and a negative polarity at the first electrode,

the second source of the alternating voltage being operative to produce a direct voltage of the low magnitude and a negative polarity at the second electrode,

the first electrode being disposed in contiguous, but spaced, relationship to the wafer.

9. (Previously Presented) In a combination as set forth in claim 7,

a first electrical conductor disposed in adjacent but spaced relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor, and

a second electrical conductor disposed in adjacent but spaced relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second electrical conductor.

10. (Original) In a combination as set forth in claim 7,

the wafer being disposed between the first and second electrodes in a substantially parallel relationship to the first and second electrodes and closer to the second electrode than the first electrode,

the wafer being at a floating potential relative to the negative potentials on the first and second electrodes and relative to the reference potential.

11. (Previously Presented) In a combination as set forth in claim 7,

the wafer being disposed in a spaced, but adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the

wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

12. (Original) In a combination as set forth in claim 10,

a vacuum pump for producing a vacuum in the enclosure, there being a space between the second electrode and the second conductive member for the flow of the molecules and ions of the inert gas from the enclosure.

13. (Previously Presented) In a combination as set forth in claim 10,

a first electrical conductor disposed in an adjacent, but spaced, relationship to the first electrode at a particular reference potential to produce a first electrical field between the first electrode and the first electrical conductor,

a second electrical conductor disposed in an adjacent, but spaced, relationship to the second electrode at the particular reference potential to produce a second electrical field between the second electrode and the second conductor,

the wafer being disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

14. (Previously Presented) In combination for etching an insulating layer in a wafer disposed in an enclosure to present a clean and fresh surface on the insulating layer for deposition,

magnetic members defining a magnetic field in the enclosure,

a first source of an alternating voltage for providing a first electrical field of a high magnitude in the enclosure,

a first electrode forming a part of the enclosure and connected to the first source of voltage for providing a negative DC voltage of a relatively high magnitude at a first position in the enclosure,

a second source of an altemating voltage for providing a second electrical field of a low magnitude in the enclosure,

a second electrode forming a part of the enclosure and connected to the second source of the alternating voltage for providing a negative DC voltage of a relatively low magnitude at a second position displaced from the first position and the wafer but near the wafer,

a conduit for introducing molecules of an inert gas into the enclosure for ionization by the combination of the electrical and magnetic fields to produce ions of high density,

the second electrode and the wafer providing a first capacitor of a high impedance, and the wafer and the ions in the enclosure providing a second capacitor of a low impedance, in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

15. (Previously Presented) In a combination as set forth in claim 14,

the first capacitor including a dielectric of the molecules and ions of the inert gas and the second capacitor including a dielectric constituting the insulating layer.

16. (Previously Presented) In a combination as set forth in claim 14,

a first electrically conductive member disposed in an adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member, and

a second electrically conductive member disposed in an adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member.

17. (Original) In a combination as set forth in claim 14,

the wafer having a floating potential and being disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode and being substantially parallel to the first and second electrodes.

18. (Previously Presented) In a combination as set forth in claim 17,

the conduit being disposed adjacent the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas being passed from the enclosure at a position adjacent to the second electrode.

19. (Previously Presented) In a combination as set forth in claim 14,

the magnetic members being disposed in a direction substantially perpendicular to the first and second electrodes to produce a helical movement of electrons in the enclosure and to provide for the production of the ions from the molecules of the inert gas by the electrons in the helical movement.

20. (Previously Presented) In a combination as set forth in claim 14,

a first electrically conductive member disposed in adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member,

a second electrically conductive member disposed in adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member,

the wafer having a floating potential and being disposed between the first and second electrodes in closer proximity to the second electrode than to the first electrode and being substantially parallel to the first and second electrodes,

the conduit being disposed adjacent, but spaced from, the first electrode to introduce the molecules of the inert gas into the enclosure and the molecules and ions of the inert gas being passed from the enclosure at a position adjacent to, but spaced from, the second electrode,

the magnetic members being disposed in a direction substantially perpendicular to the first and second electrodes to produce a helical movement of electrons in the enclosure and to provide for the production of the ions from the molecules of the inert gas by the electrons in the helical movement.

21. (Previously Presented) In combination for etching an insulating layer in a wafer to present clean and fresh surfaces on the insulating layer for deposition,

an enclosure

first and second electrodes disposed in the enclosure and displaced from each other and from the wafer for producing electrical fields in the enclosure, and

magnetic members disposed in the enclosure for producing a magnetic field in the enclosure in a direction transverse to the electrical field,

a first voltage source for producing a voltage of a high magnitude in the vicinity of the first electrode to obtain a production of a high electrical field in the enclosure,

a second voltage source for producing a voltage of a low magnitude in the vicinity of the second electrode to obtain a production of a low electrical field in the enclosure, and

a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and the magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the

insulating layer at a low rate without any pits in the surface of the insulating layer.

22. (Withdrawn) A method of etching an insulating layer in a wafer to present a clean and fresh surface on the insulation layer for a deposition on the insulating layer, including the steps of:

providing a relatively strong electrical field at first positions in an enclosure,

providing a relatively weak electrical field at second positions displaced in the enclosure from the first positions, the relatively weak electrical fields defining a capacitor with a high impedance to limit the transfer of electrical charges to the insulating layer in the wafer,

passing molecules of an inert gas through the enclosure, and

providing a magnetic field in the enclosure in a direction relative to the strong electrical field to obtain a movement of electrons in the enclosure at the positions of the strong electrical field and an ionization of molecules of the inert gas by the electrons and a movement of the ions in a direction relative to the weak electrical field to obtain a movement of the ions, in accordance with the high impedance of the capacitor defined by the relatively weak field, to the second electrode at a speed for etching the surface of the insulating layer on the wafer substantially uniformly without pitting the insulating layer.

23. (Withdrawn) A method as set forth in claim 22 wherein

the relatively strong electrical field is provided in a first direction and the relatively weak electrical field is provided in a second direction

opposite to the first direction and wherein

the magnetic field is provided in a direction transverse to the first and second directions to cooperate with the relatively strong electrical field in producing a movement of the electrons in the enclosure in a helical path for facilitating the ionization of molecules of the inert gas in the enclosure.

24. (Withdrawn): A method as set forth in claim 22

the wafer is disposed in the weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially to positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through the enclosure to positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions.

25. (Withdrawn) A method as set forth in claim 22 wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak electrical field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the capacitor and a circuit including the capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

26. (Withdrawn) A method as set forth in claim 21 wherein

the capacitor constitutes a first capacitor and wherein

the relatively weak electrical field is defined by the first capacitor and a second capacitor in a series circuit and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and in which the plates of the first capacitor are separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the first capacitor and to provide the first capacitor with the high impedance and wherein

a second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide the second capacitor with a relatively low impedance in comparison to the high impedance of the first capacitor.

27. (Withdrawn) A method as set forth in claim 26 wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low bias on the second electrode.

28. (Withdrawn) A method as set forth in claim 26 wherein

the wafer is disposed in the relatively weak electrical field and wherein

the molecules of the inert gas are passed through the enclosure initially through positions in the relatively strong electrical field to obtain an ionization of molecules of the inert gas and subsequently through positions in the relatively weak electrical field to facilitate a substantially uniform etching of the surface of the insulating layer on the wafer by the ions and wherein

the wafer is disposed in the relatively weak electrical field and wherein

an electrode providing the relatively weak field is spaced from, but disposed relatively close to, the wafer to cooperate with the wafer in providing a high impedance in the first capacitor and a circuit including the second capacitor for attracting the ions in the weak electrical field to the wafer to etch the surface of the insulating layer on the wafer without pitting the insulating layer.

29. (Withdrawn) A method as set forth in claim 26 wherein

the capacitor constitutes a first capacitor and wherein

the first capacitor and a second capacitor are in series and wherein

the first capacitor is defined by plates constituting an electrode and the wafer and wherein

the plates of the first capacitor arc separated by a space in which molecules and ions of the inert gas are disposed to define the insulator for the capacitor and to provide the high impedance and wherein

the second capacitor is defined by plates constituting the wafer and the ions of the inert gas in the enclosure and wherein the plates of the second capacitor are

separated by the insulating layer in the wafer to define the insulator of the second capacitor and to provide a relatively low impedance in comparison to the high impedance of the first capacitor and wherein

the relatively strong electrical field is provided by a first electrode and a first alternating voltage providing a relatively high negative bias on the first electrode and wherein

the relatively weak electrical field is provided by a second electrode and by a second alternating voltage providing a relatively low negative bias on the second electrode.

30. (Withdrawn) A method of etching an insulating layer on a wafer to present a clean and fresh surface on the insulating layer for deposition, including the steps of

passing molecules of an inert gas through an enclosure,

disposing a first electrode in the enclosure to provide a strong electrical field in a first direction at first positions in the enclosure to ionize molecules of the inert gas in the enclosure,

disposing a second electrode in the enclosure to provide a weak electrical field at second positions in the enclosure in a second direction opposite to the first direction,

providing a magnetic field in the enclosure, in a direction transverse to the first and second directions, to cooperate with the strong electrical field in producing charged particles in the enclosure and to cooperate with the weak electrical field in producing a transfer of the charged particles to the surface of the insulating layer in the wafer to provide a weak and controlled etching of the surface of the insulating layer without producing pits in the surface of the insulating layer.

31. (Withdrawn) A method as set forth in claim 30 wherein

the molecules of the inert gas pass through the enclosure from the strong electrical field to the weak electrical field and wherein

the magnetic field is substantially perpendicular to the strong and weak electrical fields.

32. (Withdrawn) In a combination in claim 30 wherein
the strong electrical field is defined in part by the first electrode and by an alternating voltage applied at a first magnitude to the first electrode to bias the first electrode at a negative DC potential with a first magnitude and wherein
the weak electrical field is defined in part by the second electrode and by an alternating voltage applied to the second electrode at a second magnitude less than the first magnitude to bias the second electrode at a negative DC potential with a second magnitude less than the first magnitude for producing the transfer of the charged particles to the surface of the wafer to provide the weak and controlled etching of the surface of the insulating layer without producing pits in the surface of the insulating layer.

33. (Withdrawn) In a combination as set forth in claim 30 wherein
the magnetic field is provided by magnetic members and wherein
the magnetic members and the first and second electrodes define the enclosure.

34. (Withdrawn) In a combination as set forth in claim 30 wherein
the wafer is disposed in the weak electrical field and is separated from the second electrode in the weak electrical field.

35. (Withdrawn) In a combination as set forth in claim 30 wherein
the magnetic field is substantially perpendicular to the strong and weak electrical fields and wherein
the molecules of the inert gas pass into the enclosure through the strong magnetic field and the molecules and the ions of the inert gas pass from the enclosure through the weak electrical field.

36. (Withdrawn) A method as set forth in claim 30 wherein

the second electrode and the wafer constitute plates of a first capacitor and ions and molecules of the inert gas constitute the dielectric of the first capacitor and wherein

the wafer and the ions of the inert gas constitute plates of a second capacitor and wherein the insulating layer of the wafer constitutes the dielectric of the second capacitor and wherein

the first capacitor has a higher impedance than the second capacitor.

37. (Withdrawn) A method of etching an insulating layer on a wafer having at least one socket, defined by walls in the insulating layer, to present a clean and fresh surface on the insulating layer, including the walls of the socket, for deposition, including the steps of:

passing molecules of an inert gas through an enclosure,

providing a strong electrical field at first positions in the enclosure to ionize molecules of the inert gas in the enclosure

providing a weak electrical field at second positions, including the positions of the wafer, in the enclosure, and

providing a magnetic field in the enclosure in a direction transverse to the directions of the first and second electrical fields in the enclosure to cooperate with the

strong electrical field in producing charged particles and to cooperate with the weak electrical field in producing a transfer of the charged particles, to the surface of the insulating layer in the wafer and to the walls of the socket in the insulating layer, at a low speed to provide a weak and controlled etching of a uniform thickness from the surface of the insulating layer and the walls of the socket without pitting the surface of the insulating layer or the walls of the socket.

38. (Withdrawn) A method as set forth in claim 37, including the steps of:

providing a first electrode in the enclosure for the strong electrical field and introducing an alternating voltage of a first particular amplitude to the first

electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

providing a second electrode in the enclosure for the weak electrical field and introducing an alternating voltage of a second particular amplitude less than the first particular amplitude to the second electrode to produce a weak negative DC bias on the second electrode for the creation of the weak electrical field.

39. (Withdrawn) A method as set forth in claim 37, including the steps of:

disposing the wafer in the enclosure in an adjacent but spaced relationship to the second electrode to provide a high impedance between the second electrode and the wafer for limiting the transfer of charged particles to the surface of the insulating layer and the walls of the socket and for providing for a removal of a substantially uniform

thickness from the surface of the insulating layer and from the surfaces of the walls of the socket.

40. (Withdrawn) A method as set forth in claim 37 including the steps of:

providing a first electrode to create the strong electrical field,

providing a second electrode to create the weak electrical field,

providing magnets to create the magnetic field,

the first and second electrodes and the magnets substantially defining the enclosure, and

disposing the wafer in the enclosure in a closely spaced relationship to the second electrode.

41. (Withdrawn) A method as set forth in claim 37 wherein

the wafer is at a floating potential and wherein

the magnets are substantially at a ground potential and wherein

first and second members substantially at ground potential are provided respectively in proximity to the first and second electrodes to cooperate

respectively with the first and second electrodes in creating the strong and weak electrical fields.

42. (Withdrawn) A method as set forth in claim 37 including the steps of:

introducing an alternating voltage of a first particular magnitude to the first electrode to produce a strong negative DC bias on the first electrode for the creation of the strong electrical field,

introducing an alternating voltage of a second particular magnitude less than the first particular magnitude to the second electrode to produce a weak negative bias on the second electrode for the creation of the weak electrical field, and

providing a high impedance between the second electrode and the wafer and a low impedance between the wafer and the charged particles near the wafer to produce a transfer of charged particles with limited energy to the surface of the insulating layer and the walls of the socket in the insulating layer and to provide the weak and controlled etching of the surface of the insulating layer and the walls of the socket with a substantially uniform thickness of material from the insulating layer and the wall of the socket without pitting the surface of the insulating layer or the walls of the socket.

43. (Previously Presented) In a combination as set forth in claim 21 wherein,

the first electrode provides the high electrical field in cooperation with the magnetic field for producing an ionization of molecules of an inert gas in the enclosure and wherein

the second electrode provides the low electrical field in cooperation with the magnetic field for etching the surface of the insulating layer on the wafer to obtain the smooth and uniform etching on the surface of the insulating layer at the low rate without any pits in the surface of the insulating layer.

44. (Previously Presented) In a combination as set forth in claim 21 wherein

the first voltage source applies an alternating voltage from the voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the second voltage source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

45. (Previously Presented) In a combination as set forth in claim 21 wherein

a first electrical conducting member is disposed in a cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in a cooperative relationship with the second electrode to provide for the production of the low electrical field.

46. (Previously Presented) In a combination as set forth in claim 45 wherein

the first and second electrodes are substantially parallel to the wafer and wherein

the first and second electrical conducting members are substantially parallel to the first and second electrodes.

47. (Original) In a combination as set forth in claim 46 wherein

the first and second electrical conducting members are respectively disposed in a substantially parallel, but spaced, relationship to the first and second electrodes.

48. (Previously Presented) In a combination as set forth in claim 43 wherein

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and wherein the high capacity impedance limits

the energy providing for the etching of the surface of the insulating layer in the wafer.

49. (Previously Presented) In a combination as set forth in claim 47 wherein,

the wafer and the first electrode define a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance and wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer.

50. (Previously Presented) In a combination a set forth in claim 44 wherein

a first electrical conducting member is disposed in cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the low electrical field.

51. (Previously Presented) In a combination as set forth in claim 49 wherein

the first voltage source applies an alternating voltage from the first voltage source to the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode and wherein

the second voltage source applies an alternating voltage from the source to the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode wherein

a first electrical conducting member is disposed in cooperative relationship with the first electrode to provide for the production of the high electrical field and wherein

a second electrical conducting member is disposed in cooperative relationship with the second electrode to provide for the production of the low electrical field.

X. EVIDENCE APPENDIX.

None

XI. RELATED PROCEEDING APPENDIX.

None